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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,929	07/07/2003	Shigeyuki Aino	Q76416	6920

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,929	AINO ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Final Rejection

This action is in response to an amendment filed on July 05, 2007 for the application of Aino et al., for an "Information processing apparatus" filed July 7, 2003.

Claims 19-36 are pending in the application.

Claims 19-36 are rejected under 35 USC § 102.

Claims 19-30 have been amended.

Claim 37 has been cancelled.

Claim Objections

Claims 25-30 are objected to because of the following informalities:

In claims 25-30, line 3; "another" should be changed to --other--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Horst et al. (U.S. Patent No. 5,751,932).

As per claim 19, Horst discloses an information processing apparatus (col. 10, lines 29-32) comprising:

a first computer module (Fig. 1B, element 12A), which includes a first controller (Fig. 2, element 26a) and a second computer module (Fig. 1B, element 12B), which includes a second controller (Fig. 2, element 26a), wherein:

said first computer module includes a first processor (Fig. 2, element 20b), a first main-memory and a first sub-memory (Fig. 2, elements 28, 22)

said second computer module includes a second processor (Fig. 2, element 20b), a second main-memory and a second sub-memory; (Fig. 2, elements 28, 22)

said first processor and said second processor operate execute the same instructions substantially simultaneously and are substantially synchronized with each other (col. 16, lines 19-25)

said first controller writes data to said first main-memory and said second sub-memory according to a first write request of said first processor, and at the substantially same time, said second controller writes data to said second main-memory and said first sub-memory according to a second write request of said second processor, wherein said first and second write requests are associated with the same data. Note figures 30A and 30B and col. 72, lines 55-67 through col. 73, lines 1-22, wherein Horst discloses the duplex mode, "...**Both CPUs will, in response to the instruction stream, and at essentially the same time, write the enable registers 912 of the logic element 900 of both interface units 24 of each CPU.**" Horst further discloses CPUs can access each other's

memories (col. 13, lines 1-9) "...Similarly, CPU 12A of sub-processor system 10A" may access (via two paths) memory contained in the CPU 12B of sub-processor 10B **to read or write data**."

As per claim 20, Horst discloses said first controller controls so that while said first processor and said second processor are synchronized, read access from said first processor is carried out as against said first main-memory and write access from said first processor is carried out as against said first main-memory and said second sub-memory and write access from said second processor is carried out as against said first sub- memory and said first controller controls so that, when said first processor fails to be in synchronism with said second processor, read access from said first processor is carried out as against said first sub-memory and write access from said first processor is carried out as against said first main-memory, said first sub-memory and said second sub-memory (col. 85, lines 15-46).

As per claim 21, Horst discloses said first controller copies the contents of said first sub-memory to said first main-memory when said first processor fails to be in synchronism with said second processor (Fig. 33C, element 1102) and (col. 89, lines 43-53).

As per claim 22, Horst discloses said first controller copies the contents of said first sub-memory to said first main-memory by means of a direct memory access circuit (col. 16, lines 41-47).

As per claim 23, Horst discloses said first processor computer module recovers said synchronism with said second processor when said the copy is completed for all memory areas of said first sub- memory (col. 85, lines 15-46).

As per claim 24, Horst discloses said first processor computer module recovers said synchronism with said second processor when the copying is completed for all memory areas of said first sub-memory (col. 85, lines 15-46).

As per claim 25, Horst discloses said first and second controllers are connected as a ring for three or more another computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 26, Horst discloses said first and second controllers arc connected as a ring for three or more another computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 27, Horst discloses said first and second controllers are connected as a ring for three or more another computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 28, Horst discloses said first and second controllers are connected as a ring for three or more another computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 29, Horst discloses said first and second controllers are connected as a ring for three or more another computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 30, Horst discloses said first and second controllers are connected as a ring for three or more another computer modules (Fig. 1C) and (col. 13, lines 18-39).

As per claim 31, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 32, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 33, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 34, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 35, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

As per claim 36, Horst discloses first and second computer modules are on lockstep fault tolerant computer system (col. 16, lines 19-25).

Response to Arguments

Applicant's arguments filed July 05, 2007 have been fully considered but they are not persuasive.

As per claim 19, in response to applicant's argument that "Horst does not discloses a controller, which writes data to the memory of its own computer module and the memory of another computer module according to one write request", the Examiner respectfully disagrees and would like to point out to figures 30A and 30B which illustrate the operation of the CPUs 12A and 12B in duplex mode.

Note col. 71, line 67 through col. 72, lines 1-6, wherein Horst discloses, "As FIG. 30 illustrates, the SV logic elements 900 of each interface unit 24 are connected to one another by a 2-bit SV bus 902, comprising bus lines 902a and 902b. Bus lines 902a carry one-bit values from the interface units 24 of CPU 12A to those of CPU 12B. Conversely, bus line 902b carries one-bit values from the SV logic elements 900 of CPU 12B to those of the CPU 12A."

In addition noting col. 72, lines 55-67 through col. 73, lines 1-22, wherein Horst further discloses, "...**Both CPUs will, in response to the instruction**

stream, and at essentially the same time, write the enable registers 912 of the logic element 900 of both interface units 24 of each CPU." Horst further discloses CPUs can access each other's memories (col. 13, lines 1-9) "...**Similarly, CPU 12A of sub-processor system 10A" may access (via two paths) memory contained in the CPU 12B of sub-processor 10B to read or write data**." Therefore is it apparent that when operating in duplex mode, both CPUs write data to each other's memories.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1 .136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1 .136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-4 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).